Claims

1. An overlay metrology mark for determining the relative position between two or more layers of an integrated circuit structure comprising a first mark portion associated with a first layer and a second mark portion associated with a second layer, wherein the first and second mark portions together constitute, when the mark is properly aligned, at least one pair of test zones, each test zone comprising a first mark section formed as part of the first mark portion and a second mark section formed as part of the second mark portion each comprising a plurality of elongate rectangular mark structures in parallel array adjacently disposed to form the said test zone such that the mark structures in each test zone are in alignment in a first direction within the test zone but are substantially at 90° with respect to the mark structures of at least one other test zone in alignment in a second direction, and wherein the test zones making up the or each pair are laterally displaced relative to each other along one of the said directions.

2. An overlay metrology mark in accordance with any preceding claim wherein each pair of zones are laterally disposed relative to each other such as in use to have mirror symmetry about an imaging axis of the imaging apparatus.

3. An overlay metrology mark in accordance with claim 1 wherein each mark portion is developed within or on the said layer.

4. An overlay metrology mark in accordance with claim 2 wherein each mark portion is printed on the said layer by a microlithographic process.

5. An overlay metrology mark in accordance with any preceding claim wherein each test zone has a generally square or rectangular outline shape, the rectangular directions corresponding to the said first and second directions and to the mirror axes of the imaging equipment in use.

6. An overlay metrology mark in accordance with claim 5 wherein test zones are generally square.

7. An overlay metrology mark in accordance with any preceding claim wherein only two test zones are present, and wherein the first and second mark sections of the first zone comprise closely adjacent mark structures in parallel array in a common direction, respectively part of the first mark portion and the second mark portion, the first and second mark sections of the second zone comprise similar arrays but disposed at right angles thereto, and the two test zones are laterally spaced along a line which is parallel to the direction of the test structures in one zone, and perpendicular to the direction of the test structures in the other zone.

8. An overlay metrology mark in accordance with one of claims 1 to 6 comprising more than one pair of test zones, wherein each pair is laterally disposed equidistantly about a common centre in one or other of the said two directions.

9. An overlay metrology mark in accordance with claim 8 comprising a single such pair disposed in a first direction and a single such pair in a second direction.

10. An overlay metrology mark in accordance with claim 9 wherein the first and second mark sections of each zone comprise closely adjacent mark structures in parallel array in a common direction, respectively part of the

first mark portion and the second mark portion, and wherein the first and second mark sections of two zones are in the first direction and the first and second mark sections of the other two zones in similar arrays but disposed at right angles thereto, and the two test zones in each pair are laterally spaced in respectively an X and Y direction about common centres.

11. An overlay metrology mark in accordance with any preceding claim wherein the elongate rectangular mark structures comprise single monolithic rectangular structures.

12. An overlay metrology mark in accordance with any one of claims 1 to 10 wherein the elongate rectangular mark structures comprise arrangements of substructures constituting together a general elongate rectangular outline.

13. An overlay metrology mark in accordance with claim 12 wherein the elongate rectangular mark structures comprises a row or column as the case may be of smaller constituent test structures, for example a row or column of squares.

14. An overlay metrology mark in accordance with any preceding claim wherein each elongate rectangular test structure and/or each constituent test structure comprise arrangements of design rule sized sub-structures.

15. An overlay metrology mark in accordance with claim 14 wherein the arrangements of design rule sized sub-structures are selected from parallel arrays of elongate rectangular sub-structures in either direction, arrays of square sub-structures, circles in square or hexagonal array,

arrays of holes within a suitably shaped test structure and any combinations of these or other like patterns.

16. An overlay metrology mark in accordance with any preceding claim wherein the pitch of the elongate rectangular structures is of constant period in each mark section.

17. An overlay metrology mark in accordance with claim 16 wherein the period is identical in all mark sections.

18. An overlay metrology mark in accordance with claim 16 or 17 wherein all rectangular test structures in a test zone, and preferably in the whole mark, have identical widths and spacing.

19. An overlay metrology mark in accordance with any preceding claim wherein each test structure has a width of around 0.5 to 2 μm, and wherein spacing between test structures in the array is between ½ and two structure widths.

20. An overlay metrology mark in accordance with any preceding claim wherein each mark section comprises at least five test structures in each direction.

21. A method for providing an overlay metrology mark to determine the relative position between two or more layers of an integrated circuit structure comprises the steps of:
laying down a first mark portion in association with a first layer;
and laying down a second mark portion in association with a second layer;

the first and second mark portions being so structured as to together constitute, when the mark is properly aligned, at least one pair of test zones, each test zone comprising a first mark section formed as part of the first mark portion and a second mark section formed as part of the second mark portion each comprising a plurality of elongate rectangular mark structures in parallel array adjacently disposed to form the said test zone such that the mark structures in each test zone are in alignment within the test zone, said alignment being in a first direction in half of the test zones and in a second direction substantially at 90° thereto in the other test zones, and wherein the test zones making up the or each pair are laterally displaced relative to each other along one of the said directions.

22. A method for determining the relative position between two or more layers of an integrated circuit structure:
laying down a first mark portion in association with a first layer, and laying down a second mark portion in association with a second, the first and second mark portions being so structured as to together constitute at least one pair of test zones as hereinabove described;
optically imaging the two test zones in the said first and second directions;
collecting and digitizing the image;
numerically analysing the digitized data to obtain a quantified measurement of the misalignment of the first and second mark portions.

23. The method of claim 22 wherein optical imaging of the mark is carried out using bright field microscopy.

24. The method of one of claims 21 to 23 wherein each mark portion is developed within or on the said layer.

25. The method of one of claims 21 to 24 wherein each mark portion is laid down by a microlithographic process.

26. A mark or method substantially as hereinbefore described with reference to the accompanying drawings.